wherein a first capacitance associated with one of the vertical gates is smaller than a second capacitance associated with the remaining vertical gates, and wherein a greater percentage of a voltage applied to the second or third vertical gate appears between the first vertical gate and the channel region than between the second or third vertical control gate and the first vertical gate.

REMARKS

Applicants have carefully reviewed and considered the Final Office Action mailed on October 16, 2002, and the references cited therewith.

Claims 1, 7, and 14 are amended. As a result, claims 1-23 remain pending in this application. Applicants believe that the amendments place the present Application in condition for allowance and will not necessitate a new search by the Examiner based on the remarks made by the Examiner in the Final Office Action. Moreover, the amendments are supported by the originally filed specification and not believed introduce any new matter. Accordingly, Applicants respectfully request that these amendments are proper and that they be entered in the present Application.

§103 Rejection of the Claims

Claims 1-11, 13-17, and 19-23 were rejected under 35 USC § 103(a) as being obvious over Horiguchi et al. ("A Direct Tunneling Memory (DTM) Utilizing..."). It is fundamental that in order to sustain a § 103(a) obviousness rejection, the cited references must teach, disclose, or suggest each and every element or step of the rejected claims. Applicants assert that Horiguchi fails to teach, disclose, or suggest memory cells or transistors where a greater percentage of voltage applied to a control gate appears between a floating gate and a channel region than between the control gate and the floating gate.

Applicants have previously argued that their present invention permits memory cells and transistors to be operational with much smaller voltages than as is required in Horiguchi. Applicants again assert this argument and have amended independent claims 1, 7, and 14 to more clearly point this out to the Examiner. This is so, because the floating gate capacitance is much

smaller than control gate capacitance. This capacitance difference is large enough so as to permit a greater percentage of a voltage applied to the control gate to be greater between the floating gate and a channel region than what exists between the control gate and the floating gate. As a result, the memory cells and transistors of the present invention can be programmed at lower voltages than what can be achieved with Horiguchi.

Furthermore, Horiguchi fails to teach, disclose, or suggest devices where a greater percentage of applied voltage applied to a control gate appears between a floating gate and a channel region than between the control gate and the floating gate. Thus, Applicants assert that memory cells and transistors of the present invention more efficiently use voltages applied to control gates, such that lower voltages can be used to program memory cells and transistors.

Accordingly, Applicants assert that the rejections with respect to Horiguchi are no longer sustainable and should be withdrawn. Moreover, Applicants respectfully request an indication of allowance with respect to the pending claims for the present invention.

Claims 1-23 were rejected under 35 USC § 103(a) as being obvious over Horiguchi et al. in view of Watanabe (U.S. Patent No. 6,133,601) or Hong et al. (U.S. Patent No. 5,625,213). Again, to sustain a § 103(a) obviousness rejection each and every element or step must be taught, disclosed, or suggested in the cited references. Applicants assert that none of the cited references standing alone or in combination teach, disclose, or suggest memory cells or transistors where a greater percentage of an applied voltage to a control gate appears between a floating gate and a channel region than between the control gate and the floating region.

None of the cited reference alone or in combination teach, disclose, or suggest a sufficient enough capacitance difference between a floating gate and a control gate that would permit a greater percentage of an applied voltage to the control gate to appear between the floating gate and a channel region than between the control gate and the floating gate, as is required by Applicants' amended claims 1, 7, and 14. Thus, memory cells and transistors developed with Applicants' invention can be programmed at much lower voltages than what is taught or achievable in the cited references standing alone or in combination.

Therefore, Applicants believe that the present Application is now in condition for allowance and respectfully requests and indication of the same with the present rejections

withdrawn.

CONCLUSION

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney at (612) 373-6904 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date Dec. 16, 2002 By Daniel J. Kluth
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner of Patents, Washington, D.C. 20231, on this 16 day of December, 2002.

Tina Kohout
Name

Signature